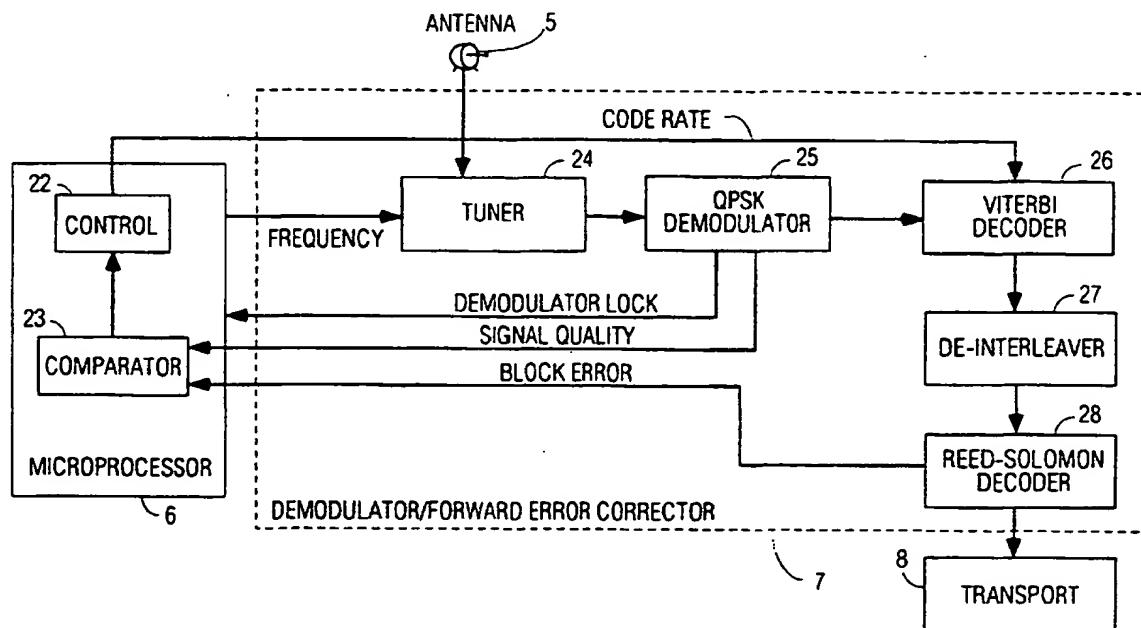




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(54) Title: SATELLITE RECEIVER CODE RATE SWITCHING APPARATUS



(57) Abstract

A satellite signal receiver (12) includes an input demodulator (7) followed by a Viterbi decoder (26) and a Reed-Solomon decoder (28). A received signal is encoded with information including error-representative information, and exhibits an error correction code rate which is a function of the power level of a satellite transmitted signal. The demodulator (7) produces control signals representing the presence or absence of synchronism with the received signal, and signal quality (e.g. signal-to-noise ratio). The Reed-Solomon decoder (28) produces a control signal indicating whether or not error detection and correction is occurring properly. These control signals are sensed by a control network to change the code rate of the Viterbi decoder if necessary.

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SATELLITE RECEIVER CODE RATE SWITCHING APPARATUS

This invention is related to the field of digital satellite
5 communication systems, and more particularly to error correcting
apparatus in a receiver in such a system.

BACKGROUND OF THE INVENTION

Currently, a satellite may receive a signal representing
10 audio, video or data information from a transmitter. The satellite
amplifies and broadcasts this signal to a receiver via a
communication channel at a specified frequency and bandwidth.
Since communications channels are subject to errors due to noise
within the channel itself and to external sources, error correction
15 is desirable. One technique for reducing or eliminating errors is
Forward Error Correction (FEC). This technique sends a certain
amount of extra information along with the original information.
When errors occur, the receiver uses the extra information to
locate and correct errors without further communication with the
20 transmitter.

Two widely used types of forward error correction systems
employ convolutional coding and block coding. Convolution coding
operates on a continuum of data which is serially and
continuously conveyed to an encoder. A convolutional encoder
25 analyzes the current data and some amount of previous data. The
encoder adds error correction data to the current data, thereby
creating a new data signal. The system then outputs a continuous
stream of the new data at a higher rate, either more data being
transmitted faster, or more data over a longer time period. The
30 receiver is conditioned to analyze a signal encoded with the
convolutional error coding method used by the transmitter.

Block coding, such as Reed-Solomon coding, encodes the data
signal with additional error correcting data using a specified
algorithm. In a Reed-Solomon encoder, data is typically divided
35 into equal sized units or blocks of a convenient size. Using a Reed-
Solomon algorithm, these blocks have data added to them in some

2

manner that is dependent upon the data itself. This process creates a new block of somewhat larger size that may or may not resemble the original data. However, by the receiver understanding the coding scheme used, the new block of data may be analyzed and the original data extracted, even if errors have been created in the data.

Each type of error coding has an associated code rate based on the number of bits entering the encoder divided by the number leaving it. Thus if 750 bits of data enter, 250 bits of error correction code are added, and 1000 bits (750 + 250) are output, the code rate is said to be a $3/4$ (750/1000) code rate, and the apparatus is said to run at a $3/4$ error correction coding rate. This is sometimes referred to as rate $3/4$ forward error correction.

These same rates designate the error decoding rate used by a decoder, although the reverse operation is performed. For example, 1000 bits of data may be input, 250 of which are error correction code and the remaining 750 bits are data. The 250 bits of error correction code are removed from the data signal and used to detect and correct errors in the data signal. The remaining 750 bits of data are output. The decoder is said to run at a $3/4$ error correction decoding rate.

The amount of error correcting information encoded into a data signal may depend, in part, on the operation of the satellite. For example, a satellite broadcast system may operate in two power modes, low and high. At high power, the signal received and transmitted by the satellite is stronger. As a result, the quality of a received signal is improved, and less error correction coding is required to obtain a desired data quality. For example, at high power, transmitted data may be approximately 25% error correction data and 75% usable data. Similarly, when the satellite operates at low power, the signal transmitted and received is weaker. Additional error correction data is therefore required to achieve the desired data quality. For example, at low power, approximately 40% of the transmitted data is error correction data and approximately 60% is usable data.

A desirable error correction coding rate will maximize the usable data and minimize the error correction data transmitted. If insufficient error correction data is included in the transmitted signal, the signal will not be received reliably, if at all, by the receiver. If excessive error correction data is included, the signal will be received correctly, but a lesser percentage of the output signal will be available for real data than if the error correction data had been matched to the transmitting power of the satellite.

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SUMMARY OF THE INVENTION

In accordance with the principle of the present invention, it is herein recognized that it is desirable to match the rate of error correction coding to the differing power levels of a satellite. Accordingly, error correction coding rates are a function of differing power levels of the satellite, which coding rate may change without direct notification to a receiver. A receiver senses that the error correction code rate has been altered at the transmitter, and in response alters the error correction decoding rate used by the receiver.

20

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIGURE 1 is a block diagram of a satellite transmitting/receiving system including apparatus according to the invention.

FIGURE 2 is a block diagram of a portion of the receiver in FIGURE 1, including a demodulator/forward error correction unit in accordance with the invention.

FIGURE 3 is a flowchart to aid in understanding a sequence of events which occur in controlling the apparatus shown in FIGURE 2.

FIGURE 4 is a flowchart to aid in understanding another sequence of events which occur in controlling the apparatus of FIGURE 2.

DETAILED DESCRIPTION OF THE DRAWINGS

The system of FIGURE 1 includes a transmitter 1 which processes a data signal from a source 14 (e.g., television signal source) and transmits it to a satellite 13 which receives and re-broadcasts the signal to a receiver 12. Transmitter 1 includes an encoder 2, a modulator/forward error corrector (FEC) 3, and an uplink unit 4. Encoder 2 compresses and encodes signals from source 14 according to a predetermined standard such as MPEG. (MPEG is an international standard developed by the Moving Pictures Expert Group of the International Standards Organization for coded representation of moving pictures and associated audio stored on digital storage medium.) An encoded signal from unit 2 is supplied to modulator/Forward Error Corrector (FEC) 3, which encodes the signal with error correction data, and Quaternary Phase Shift Key (QPSK) modulates the encoded signal onto a carrier. Both convolutional and RS block coding are performed in block 3.

Uplink unit 4 transmits the compressed and encoded signal to satellite 13, which broadcasts the signal to a selected geographic reception area. In this embodiment, satellite 13 operates in two modes, which trade off channel capacity and transmission power. In the first mode, satellite 13 illustratively transmits 16 channels at 120 watts each. In the second mode, satellite 13 transmits 8 channels at 240 watts each.

The signal from satellite 13 is received by an antenna 5 coupled to an input of a so-called set-top receiver 12, e.g., an interface device situated atop a television receiver. Receiver 12 includes a demodulator/Forward error correction (FEC) decoder 7 to demodulate the signal and to decode the error correction data, a microprocessor 6 which operates interactively with demodulator/FEC 7, and a transport 8 to transport the signal to an appropriate decoder within unit 9 depending on the content of the signal, i.e., audio or video information. Transport unit 8 receives corrected data packets from unit 7 and checks the header of each packet to determine its routing. Decoders in unit 9 decode the

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signal and remove added transport data if used. An NTSC Encoder 10 encodes the decoded signal to a format suitable for use by signal processing circuits in a standard NTSC consumer television receiver 11.

5 Referring now to FIGURE 2, demodulator/FEC unit 7 acquires, demodulates, and decodes the data signal which is received from antenna 5. This unit includes a tuner 24, a Quaternary Phase Shift Keyed (QPSK) demodulator 25, a Viterbi convolutional decoder 26, a de-interleaver 27, and a Reed-
10 Solomon (RS) decoder 28, all of conventional design, arranged as shown.

Tuner 24 receives an input signal from antenna 5. Based upon a user's channel selection, a control unit 6, e.g., a microprocessor, sends a Frequency signal to tuner 24. This signal
15 causes tuner 24 to tune to the appropriate channel and to frequency downconvert the received signal in response to the tuning frequency sent to tuner 24 from microprocessor 6. An output signal from tuner 24 is provided to QPSK demodulator 25.

QPSK demodulator 25 locks onto (synchronizes with) the
20 tuned channel, demodulates the modulated data signal, and generates a signal indicative of the quality of the demodulated signal. Demodulator 25 demodulates the modulated input data signal regardless of the error correction code rate of the received data signal. Phase locked loop circuitry in demodulator 25
25 synchronizes the operation of demodulator 25 with the input signal using well known techniques. Demodulator 25 generates a Demodulator Lock output control signal that indicates whether or not demodulator 25 is synchronized with the input signal, and supplies this signal to a storage register in microprocessor 6. An
30 output demodulated data signal from unit 25 is provided to Viterbi decoder 26. Demodulator 25 also generates an output Signal Quality signal. This signal represents the quality of the signal received from the satellite transmission, and is related to the signal-to-noise ratio of the received signal. Various sources of
35 noise, as well as rain fade, may impair the quality of a received signal. A QPSK demodulator suitable for use as unit 25 is

6

commercially available from Hughes Network Systems of Germantown, MD (integrated circuit type No. 1016212), and from Comstream Corp., San Diego, California (No. CD2000).

Decoder 26 uses a Viterbi algorithm to decode and to correct 5 bit errors in the demodulated signal from unit 25. Decoder 26 includes internal networks, as known, to synchronize its operation to the incoming demodulated signal in order to effectively decode the demodulated signal.

Decoder 26 operates at one of two error correction decoding 10 rates, which correspond to error correction coding rates provided at the transmitter. When satellite 13 operates in the low power mode, the transmitted signal uses a rate 2/3 error correction code. When satellite 13 operates in the high power mode, the 15 Rate control signal developed by control unit 22 in microprocessor 6 indicates which error correction code rate decoder 26 should use. The Code Rate control signal may be a binary signal with one logic level signifying that the code rate used by unit 26 should remain unchanged, and another logic level causing unit 26 to 20 switch to another programmed code rate. The Code Rate control signal is provided by a block 22 in response to an output from a digital comparator 23. Comparator 23 provides an output logic state as a function of the logic state of input control signals, e.g., Signal Quality and Block Error, as will be discussed. These signals 25 are applied to storage registers which are monitored by comparator 23. After decoder 26 decodes and error corrects the demodulated data signal, the decoded data signal is supplied to a de-interleaver 27. De-interleaver 27 restores the ordering of the data signal to its original sequence, and forms Reed-Solomon 30 blocks (RS blocks), in accordance with known techniques. For this purpose de-interleaver 27 relies upon an 8-bit sync word inserted by the encoder at the beginning of each RS block, thereby providing RS block synchronization. The de-interleaved signal is supplied to a Reed-Solomon (RS) decoder 28. 35 RS decoder 28 decodes the RS blocks and corrects byte errors within the block, using a decode rate of 130/146, for

example. The 8-bit sync byte word appended to each Reed-Solomon block facilitates locating the beginning of each Reed-Solomon block. An effective RS decode rate of 130/147 results from the use of the appended sync word. This 8-bit sync byte word is removed by de-interleaver 27 before Reed-Solomon decoding, so that only 146 bytes per block are RS decoded.

RS decoder 28 also provides error detection when the number of errors in a block exceeds the correction capability of the RS code. For example, RS decoder 28 may correct up to eight byte errors within a block. If more than eight byte errors are detected, RS decoder 28 produces an output Block Error signal with, e.g., a binary signal with a high logic level to indicate that more errors exist than can be corrected. An uncorrectable RS block is discarded and not used. If an RS block is RS decodable within the prescribed eight byte parameters, the decoded signal is supplied to transport unit 8. The disclosed combination of a Viterbi algorithm convolutional decoder followed by an RS block decoder has been found to produce very good error detection/correction results, particularly in the error rate and signal-to-noise environment commonly associated with satellite transmissions.

The transmitter (unit 3 in FIGURE 1) may change the error correction code rate at any time without notifying receiver demodulator/decoder 7 of the change. In this example, the system supports two (Viterbi and RS) error correction code rates: $2/3 \cdot 130/147$ at low satellite power, and $6/7 \cdot 130/147$ at high satellite power. When the power mode is switched, the error correction code rate may be switched. Since the error correction coding rate of RS decoder 28 at the receiver remains constant (130/147), only the Viterbi decoder error correction decoding rate need be altered by switching from one programmed rate to another ($2/3$ to $6/7$ or vice-versa). The error correction decoding rate used by Viterbi decoder 26 is altered through use of the Code Rate control signal supplied by microprocessor 6. Microprocessor 6 establishes the state of the Code Rate signal in response to the state of the Block Error signal from RS decoder 28. Microprocessor

6 may also respond to a signal from demodulator 25 to determine the state of the Code Rate signal, as will be discussed.

Various conditions may cause the receiver error correction decode rate to be uncertain. For example, when the system is
5 operating using one error correction decode rate, the rate may be switched at the transmitter or the channel changed to a channel for which the error correction rate is not known. In accordance with the invention, the use of an incorrect error correction decode rate is detected, and the error correction decode rate is changed.
10 This may be achieved by analyzing the success of decoding by RS decoder 28 as indicated by the Block Error signal. This may also be achieved by analyzing the quality of the data signal, as determined by QPSK demodulator 25, relative to the success of RS decoding as determined by the Block Error signal from RS decoder
15 28. In each case, demodulator 25 synchronizes itself to the incoming data signal. The power level of a received satellite signal and the error correction coding rate are transparent to demodulator 25. Demodulator 25 will therefore always attempt to demodulate the received data signal, and supply the demodulated
20 signal to Viterbi decoder 26.

A decoded signal from Viterbi decoder 26 is provided to RS decoder 28 via de-interleaver 27. If decoder 26 uses the proper error correction decode rate to decode the data signal, de-interleaver 27 and Reed-Solomon decoder 28 will operate
25 normally. In such case the Block Error signal will exhibit a given state, e.g., a logic "low" level, indicating normal decoding. If decoder 26 is using an incorrect error correction code rate for a given input signal, it is unlikely that decoder 28 will provide a normal output. In such case the Block Error signal will exhibit a
30 different state, e.g., a logic "high" level, to signify an abnormal output from RS decoder 28. In each case, the Block Error signal is analyzed to determine if the error correction code rate used by Viterbi decoder 26 should be changed.

FIGURE 3 is a flow chart which illustrates a sequence of
35 events occurring at the receiver when, for example, the error correction code rate is changed at the transmitter. This change

may cause a perturbation to appear in the transmitted data signal because of the modulator switching to the new error correction code rate. A perturbation may also occur due to rain fade, or tuning to a new channel. Such a perturbation may cause the QPSK demodulator at the receiver to lose synchronization with the data signal.

Considering FIGURE 3 with FIGURE 2, when demodulator 25 loses synchronization (lock) with the data signal, logic circuits in demodulator 25 generate, e.g., a high logic level Demodulator Lock signal (step 31) to indicate the loss of synchronization.

Demodulator 25 attempts to re-synchronize with the input data signal until the data signal is strong enough for proper reception (steps 32 and 33). When demodulator 25 regains synchronization, the Demodulator Lock signal exhibits a low logic level to indicate that synchronization has been acquired. Viterbi decoder 26 is then set to a default error correction code rate (step 34) by microprocessor 6, through use of the Code Rate signal. The default code rate is a pre-programmed one of the available code rates.

When demodulator 25 loses synchronization with the data signal, synchronization circuitry associated with Viterbi decoder 26 typically will be unable to synchronize with the signal from the output of the demodulator. As a result, incorrect information will be provided to the core of the Viterbi decoder, and the Viterbi decoder will output an abnormal signal. In such case demodulator 25 will be unable to locate and use the inserted 8-bit sync word for aligning the RS blocks. RS decoder 28 therefore will be unable to properly decode the output signal from Viterbi decoder 26, and the level of the Block Error signal will indicate improper decoding by RS decoder 28.

A predetermined period of time after demodulator 25 has regained synchronization, microprocessor 6 will examine the Block Error signal (step 35). If the Block Error signal state (low) indicates normal decoding, the (default) error correction code rate being used by Viterbi decoder 26 is assumed to correspond to the transmitted code rate (step 39). Alternatively, if the Block Error signal exhibits another state (high) indicating abnormal decoding,

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the error correction code rate of Viterbi decoder 26 is assumed to be incorrect, since if Viterbi decoder 26 is using an incorrect error correction coding rate, RS decoder 28 is unlikely to be able to provide normal RS block decoding. Microprocessor 6 then
5 provides a Code Rate signal with a state indicating that the error correction code rate of Viterbi decoder 26 should be changed (step 37).

The Block Error signal is checked at predetermined intervals by comparator 23 of microprocessor 6. The Viterbi error
10 correction code rate will be switched between the available error correction code rates until the Block Error signal exhibits a state indicating that the data signal is being normally decoded.

Tuning to a new channel may not necessarily result in demodulator 25 losing synchronization. If synchronization is lost
15 during a channel change, the process described above involving steps 35, 37 and 39 will be repeated.

As another example, the Signal Quality signal from QPSK demodulator 25 may be used to determine if the wrong error correction code rate is being used by Viterbi decoder 26. FIGURE
20 4 (considered with FIGURE 2) illustrates the sequence of events which occur in this case. In FIGURE 4, steps 44, 45 and 49 respectively correspond to steps 34, 35 and 39 in FIGURE 3. FIGURE 4 differs in that steps 46, 47 and 48 have been added.

When QPSK demodulator 25 initially achieves
25 synchronization (lock) with the data signal, Viterbi decoder 26 is set to a default code rate (step 44) as discussed. Viterbi decoder 26 then attempts to synchronize itself with the demodulated data signal. If synchronization is achieved, de-interleaver 27 and RS decoder 28 receive a decodable signal. RS decoder 28 then
30 generates a low level Block Error signal to indicate proper decoding (step 45). Microprocessor 6 senses the low level Block Error signal, and determines that the proper error correction code rate is being used by the Viterbi decoder (step 49).

In contrast, if Viterbi decoder 26 is unable to synchronize
35 with the data signal, de-interleaver 27 and RS decoder 28 receive an undecodable data signal from Viterbi decoder 26. De-

11

interleaver 27 and RS decoder 28 will then be unable to operate properly upon the data signal, and RS decoder 28 will generate a high level Block Error signal representing this condition.

Microprocessor 6 senses (via comparator 23) the Signal Quality
5 signal supplied by the QPSK demodulator (step 46). If the level of the Signal Quality signal is high, indicating that RS decoder 28 should have been able to decode the data signal, then microprocessor 6 generates a Code Rate signal instructing Viterbi decoder 26 to switch error correction code rates (step 47).

10 If the level of the Signal Quality signal is low, indicating that the RS decoder could not produce a sufficiently decoded signal even if Viterbi decoder 26 were using the proper error correction coding rate, microprocessor 6 will not cause a change in the error correction code rate of Viterbi decoder 26. This condition may
15 occur as a result of a rain fade, for example. Microprocessor 6 then waits a specified period of time (step 48) before sampling the Block Error signal, to allow decoder 26 time to synchronize itself at the current error correction code rate. If the Block Error signal remains at a high level (indicating improper decoding),
20 microprocessor 6 will again sample the Signal Quality signal. Microprocessor 6 will sample the Block Error signal several times at predetermined intervals until proper decoding is indicated by the Block Error signal. As shown in FIGURE 4, microprocessor 6 will continue sampling both the Block Error signal and the Signal
25 Quality signal, and will instruct Viterbi decoder 26 to change the error correction code rate or to wait a specified period of time until the Block Error signal exhibits a low level, indicating proper decoding.

The following table summarizes the conditions described above with respect to the possible states (levels) of the Signal Quality and Block Error control signals.

5

<u>Signal Quality</u>	<u>Block Error</u>	<u>Comments</u>
HIGH	LOW	Normal Operating condition
10 LOW	LOW	Correct code rate; poor signal
LOW	HIGH	Undetermined cause (rain fade); wait
15 HIGH	HIGH	Incorrect code rate; switch code rate

Viterbi decoder 26 may operate in response to more than two error correction code rates, depending upon the requirements of a particular system. Similarly, the described control signals could indicate a particular state or value with a high or a low logic level. Encoder and decoder networks other than Viterbi and Reed-Solomon may be used in apparatus incorporating the invention.

WHAT IS CLAIMED IS:

1. In a data communication system for processing an input signal encoded with information including information to facilitate error correction at a decoder, decoder apparatus comprising:
 - input means (5, 24, 25) for receiving said encoded input signal;
 - first decoder means (26) responsive to an output signal from said input means and operating at a first error correction code rate;
 - means (28) for providing a first control signal (Block Error) representative of normal or abnormal decoding by said first decoder means; and
 - control means (6, 22, 23) responsive to said first control signal for altering said first error correction code rate as a function of the state of said first control signal.
2. Apparatus according to claim 1, wherein said first control signal alters said first error correction rate when said first control signal represents abnormal decoding by said first decoder means.
3. Apparatus according to claim 1, wherein said system is a satellite broadcasting system subject to transmitting a signal at different power levels with respectively associated different error processing code rates.
4. Apparatus according to claim 1, wherein said providing means comprises second decoder means responsive to an output signal from said first decoder means and operating at a second error correction code rate.

5. Apparatus according to claim 1, wherein said input means includes means (25) for producing a second control signal (Demod. Lock) indicative of said apparatus being synchronized with said input signal; and wherein said control means responds to said first and second control signals for altering said first code rate.
- 10 6. Apparatus according to claim 5, wherein said input means includes means for demodulating (25) said input signal; and wherein said second control signal is indicative of synchronization of said demodulating means with said input signal.
- 15 7. Apparatus according to claim 6, wherein said control means alters said first code rate when said second control signal indicates that said demodulating means is unsynchronized.
- 20 8. Apparatus according to claim 1 wherein said control means is additionally responsive to a second control signal, (Signal Quality) indicative of the signal quality of said input signal, for altering said first code rate when said second control signal represents an unacceptable signal quality.
- 25 9. Apparatus according to claim 5 wherein said control means is additionally responsive to a third control signal, (Signal Quality) indicative of the signal quality of said input signal, for altering said first code rate when said third control signal indicates an unacceptable signal quality value.
- 30

10. Apparatus according to claim 6 wherein
said control means is additionally responsive to a third
control signal, (Signal Quality) indicative of the signal quality of
5 said input signal, for altering said first code rate when said third
control signal indicates an unacceptable signal quality value.

11. Apparatus according to claim 1, wherein
said first decoding means is a convolutional decoder.
10

12. Apparatus according to claim 11, wherein
said convolutional decoder is a Viterbi decoder.

13. Apparatus according to claim 4, wherein
said second decoding means is a block decoder.
15

14. Apparatus according to claim 13, wherein
said block decoder is a Reed-Solomon decoder.

20 15. In a data communication system for processing an input
signal encoded with information including information to facilitate
error correction at a decoder, decoder apparatus comprising:
input means (5, 24, 25) for receiving said encoded input
signal;

25 means (26) for decoding an output signal from said
input means using a changeable error correction code rate;
means (25) for producing a control signal (Demod. Lock)
indicative of synchronization of said apparatus with said encoded
data signal; and

30 control means (6, 22, 23) responsive to said control signal
for altering said code rate as a function of the state of said control
signal.

16. Apparatus according to claim 15, wherein:
said control means alters said code rate in the presence of
an unsynchronized condition; and
5 said system is a satellite transmission system.

17. In a data communication system for processing an input
signal encoded with information including information to facilitate
error correction at a decoder, decoder apparatus comprising:
10 means (26) for decoding an output signal from said
input means using a changeable error correction code rate;
means (25) for producing a control signal (Signal Quality)
indicative of signal quality of said input signal; and
control means (6, 22, 23) responsive to said control signal
15 for altering said code rate as a function of the state of said control
signal.

18. Apparatus according to claim 18, wherein:
said control means alters said code rate when said control
20 signal indicates unacceptable signal quality.

1/4

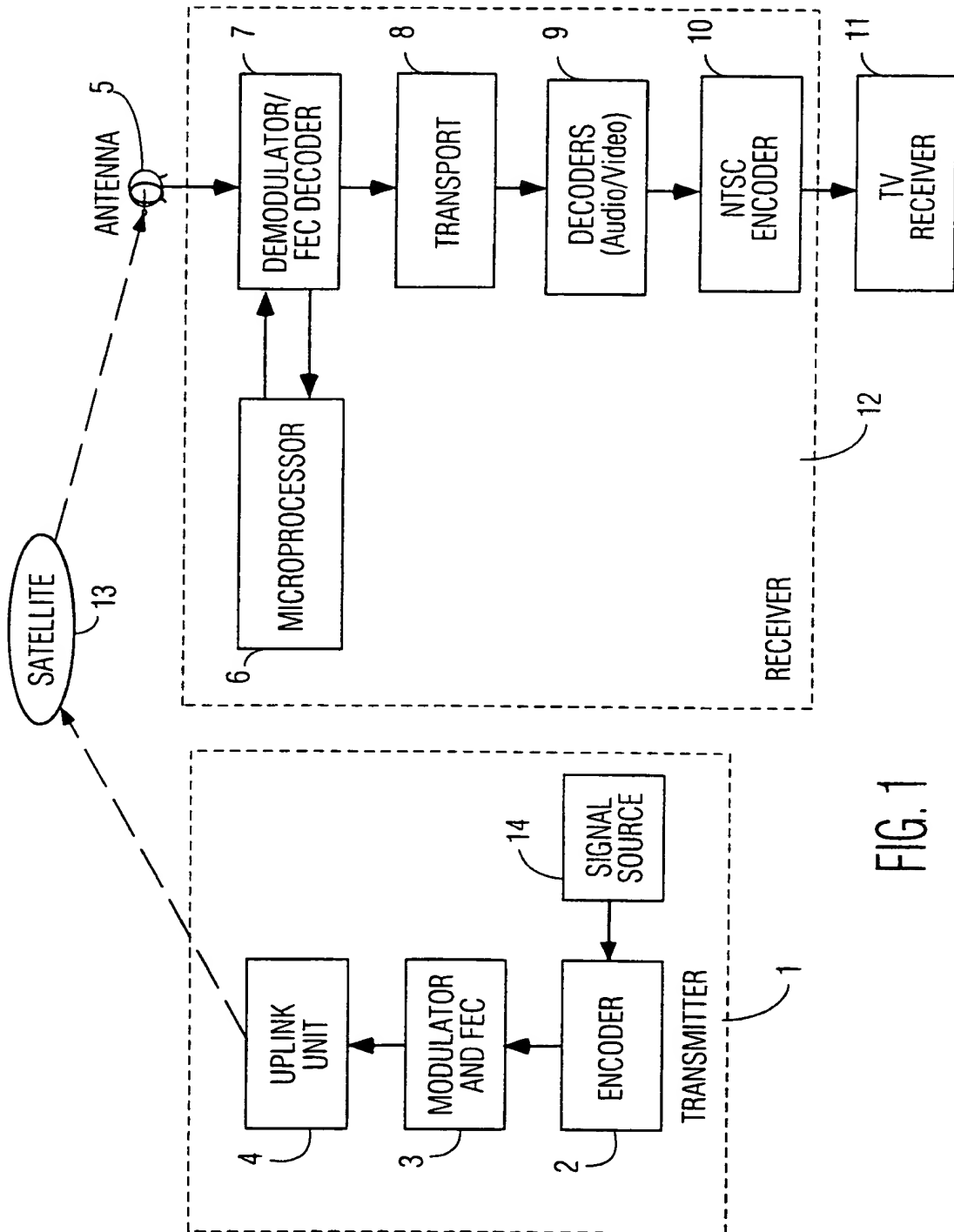


FIG. 1

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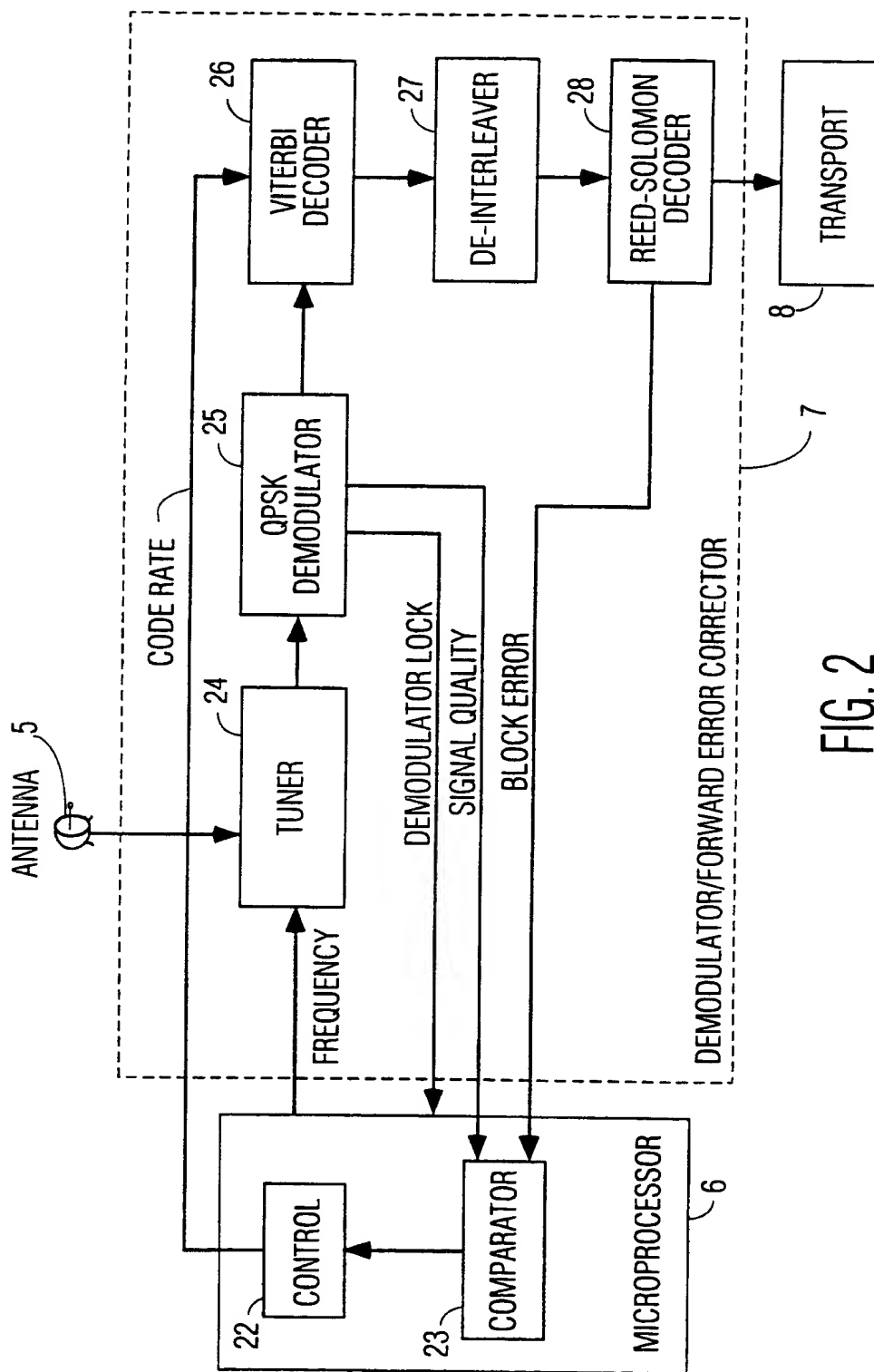


FIG. 2

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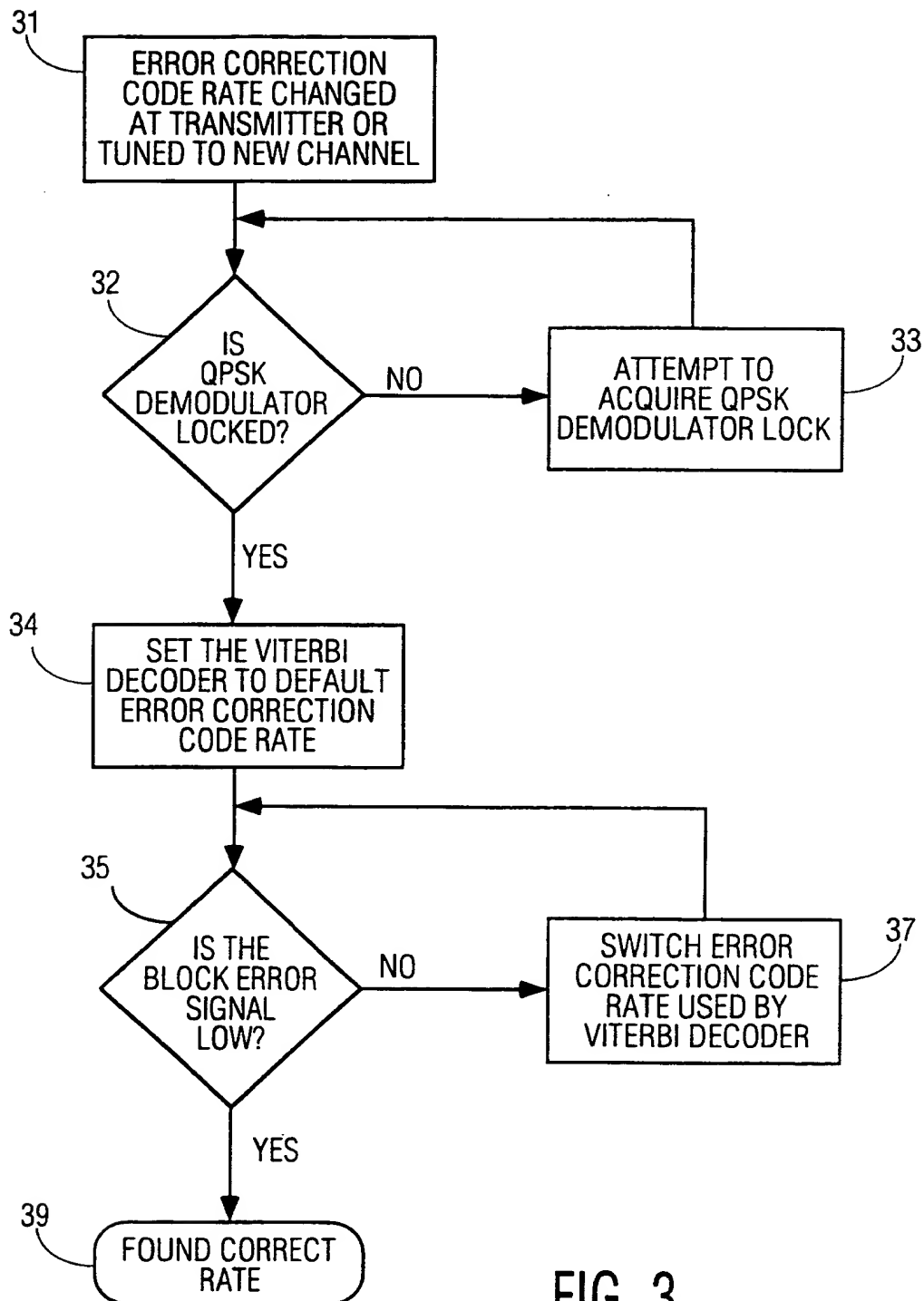


FIG. 3

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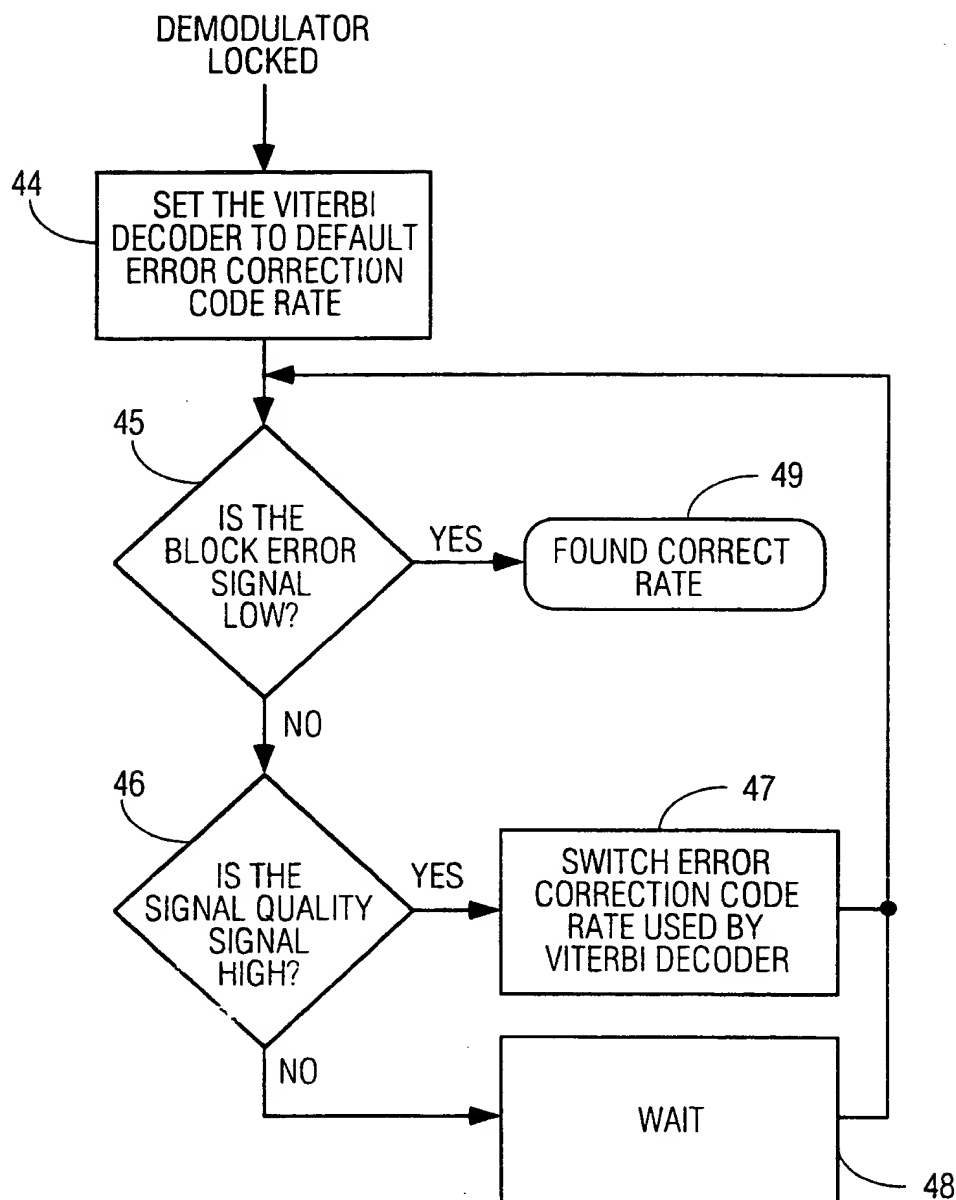


FIG. 4

INTERNATIONAL SEARCH REPORT

ational application No.

T/US93/11338

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H03M 13/00; G06F 11/10

US CL : 371/35.41 43

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 371/35.41 43

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, PROQUEST (IEEE ON DISK)

SEARCH TERMS: ADAPTIVE DECODING, CODE RATE, VARIABLE RATE, VITERBI DECODER

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	IEEE Transactions on Communications vol.40, no. 1 Jan. 1992 Pursley, Michael et al, "Variable Rate Hybrid ARQ for Meteor-Burst Communications", Parts I-III (part IIIc. pp 65-67)	1-18
Y	IEEE Journal on Selected Areas in Communications, Vol.10, no. 2, Feb. 1992, Kim, Snag Wu, "Frequency-Hopped Spread-Spectrum Random Access with Retransmission Cutoff and Code Rate Adjustment", pp 344-345 parts I-II.	1,15,17
Y	USA 5,151,904 (Reiner et al) 29 September 1992 column 2 line 8 to 62 and column 5 line 8 to column 8 line 9.	1,15,17

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	USA 4,047,151 (Rydbeck et al) 06 September 1977 Column 4 line 62 to column 5 line 35, and column 7 line 4 to column 8 line 62, and column 11 line 11 to column 13 line 69.	1-18
Y	USA 5,157,672 (Kondou et al) 20 October 1992 Abstract	1,3,15,17
Y	USA 4,901,319 (Ross) 13 February 1990 Abstract and columns 1-2.	1,15,17

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